SSC8P20AN3

N-Channel Enhancement Mode MOSFET with PNP Transistor

➢ Features

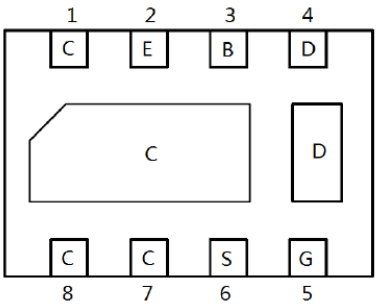
N-Channel:

V_{DS}	V_{GS}	R_{DSON} Typ.	I_D
20V	±8V	200mΩ@4V5	0.8A
		250mΩ@2V5	

PNP Transistor:

V_{CB}	V_{CE}	V_{EB}	V_{CESAT} Typ.	I_C
-40V	-40V	-6V	-180mV	-1A

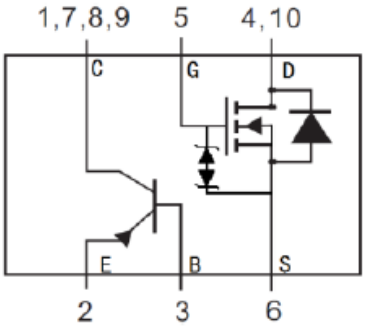
➢ Pin configuration



DFN3X2-8L (Bottom View)

➢ Description

The SSC8P20AN3 combines an N-Channel enhancement mode power MOSFET which is produced with high cell density and a Media Power PNP Transistor. The tiny and thin outline saves PCB consumption.



Circuit Diagram

➢ Applications

- Power management
- Charging circuits
- Li-Battery Charging
- Power switches

Marking (Top View)

➢ Ordering Information

Device	Package	Shipping
SSC8P20AN3	DFN3x2-8L	3000/Reel

➢ Absolute Maximum Ratings (T_A=25℃ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
N-MOS			
V_{DSS}	Drain-to-Source Voltage	20	V
V_{GSS}	Gate-to-Source Voltage	±8	V
I_D	Continuous Drain Current	0.8	A
I_{DM}	Pulsed Drain Current	3	A
PNP Transistor			
V_{CBO}	Collector-Base Voltage	-40	V
V_{CEO}	Collector-Emitter Voltage	-40	V
V_{EBO}	Emitter-Base Voltage	-6	V
I_C	Collector Current	-1	A
I_{CM}	Pulsed Collector Current	-2	A
Power Dissipation and Temperature			
P_D	Power Dissipation [a]	2.1	W
T_A	Operation Temperature Range	-40 to 85	℃
T_L	Lead Temperature	260	℃
T_J	Operation Junction Temperature	-55 to 150	℃
T_{STG}	Storage Temperature	-55 to 150	℃

➢ Thermal Resistance Ratings (T_A=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Junction-to-Ambient Thermal Resistance [a]	$R_{\theta JA}$	45	℃/W

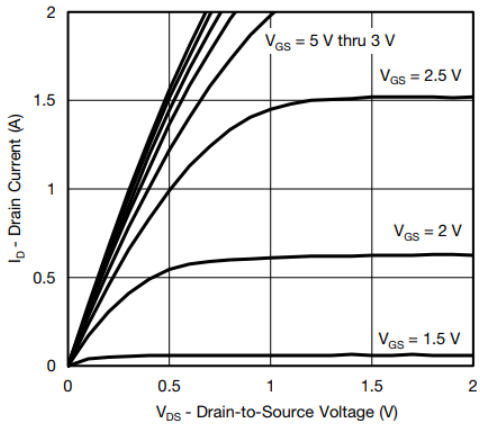
Note:

a. The value of $R_{\theta JA}$ is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The Power dissipation PD is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

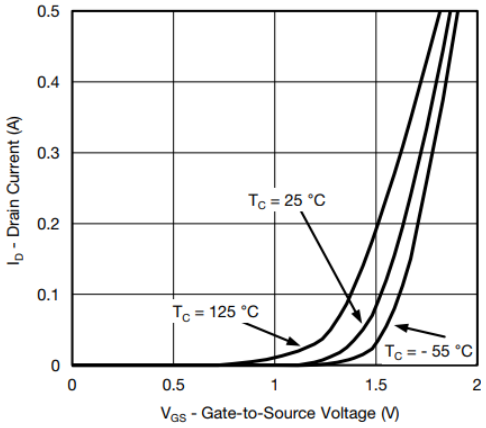
➢ Electrical Characteristics (T_A=25℃ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
N-Channel Enhancement Mode MOSFET						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =250uA	20			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250uA	0.35	0.6	1	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 4.5V, I_D = 0.5A		200	600	mΩ
		V_{GS} = 2.5V, I_D = 0.5A		250	850	
		V_{GS} = 1.8V, I_D = 0.35A		350	950	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16V, V_{GS} = 0V			1	μA
Gate-Source leak current	I_{GSS}	V_{GS} = ±8V, V_{DS} = 0V			±10	μA
Forward Voltage	V_{SD}	V_{GS} = 0V, I_S = 1A			1.3	V
Transconductance	G_{FS}	V_{DS} = 5V, I_D = 0.5A		2.2		s
Input Capacitance	C_{ISS}	V_{DS} =16V, V_{GS} = 0V, f = 200kHz		130		pF
Output Capacitance	C_{OSS}			20		
Reverse Transfer Capacitance	C_{RSS}			16		
Turn-on Delay Time	$T_{D(ON)}$	V_{DS} = 6V, V_{GS} = 4.5V, R_L = 6Ω, R_G = 6Ω, I_D = 0.8A		6		ns
Turn-on Rise Time	Tr			23		
Turn-off Delay Time	$T_{D(OFF)}$			42		
Turn-off Fall Time	Tf			78		
PNP Transistor						
Collector-Base Breakdown Voltage	BV_{CBO}	I_C = -50μA, I_E = 0	-40			V
Collector-emitter Breakdown Voltage	BV_{CEO}	I_C = -1mA, I_B = 0	-40			V
Emitter -Base Breakdown Voltage	BV_{EBO}	I_E = --50μA, I_C = 0	-6			V
Collector Cutoff Current	I_{CBO}	V_{CB} = -20V, I_E = 0			-0.1	μA
Emitter Cutoff Current	I_{EBO}	V_{EB} = -4V, I_C = 0			-0.1	μA
DC Current Gain	h_{FE}	V_{CE} = -2V, I_C = -0.5A	100		360	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = -0.8A, I_B = -80mA		-0.18	-0.5	V
Base-Emitter Saturation Voltage	$V_{BE(sat)}$	I_C = -0.8A, I_B = -80mA			-1.2	V
Transition frequency	f_T	V_{CE} = -6V, I_C = -20mA, f=30MHz	150			MHz

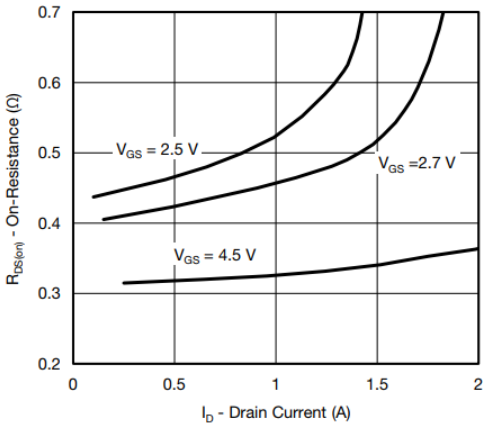
➢ N-Channel Typical Performance Characteristics (T_A=25℃ unless otherwise noted)



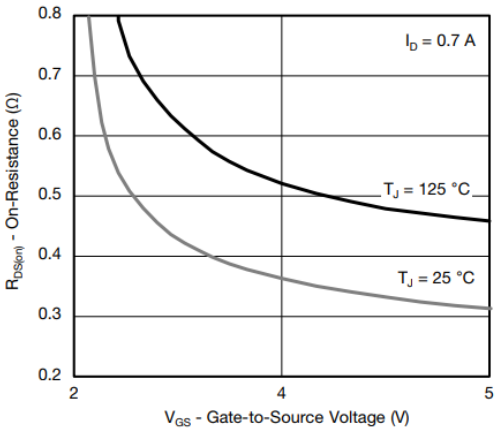
Output Characteristics



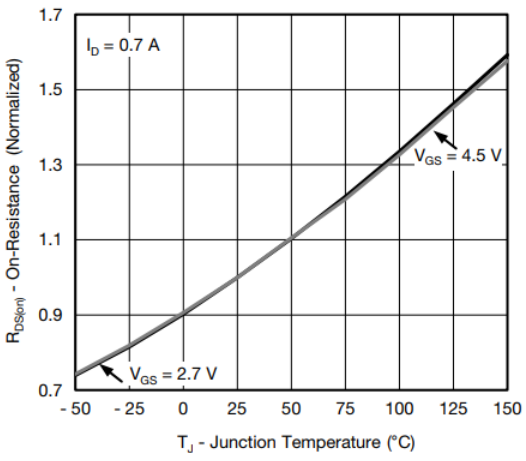
Transfer Characteristics



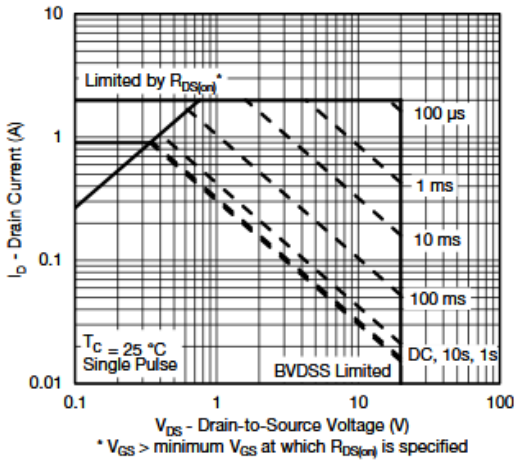
On-Resistance vs. Drain Current and Gate Voltage



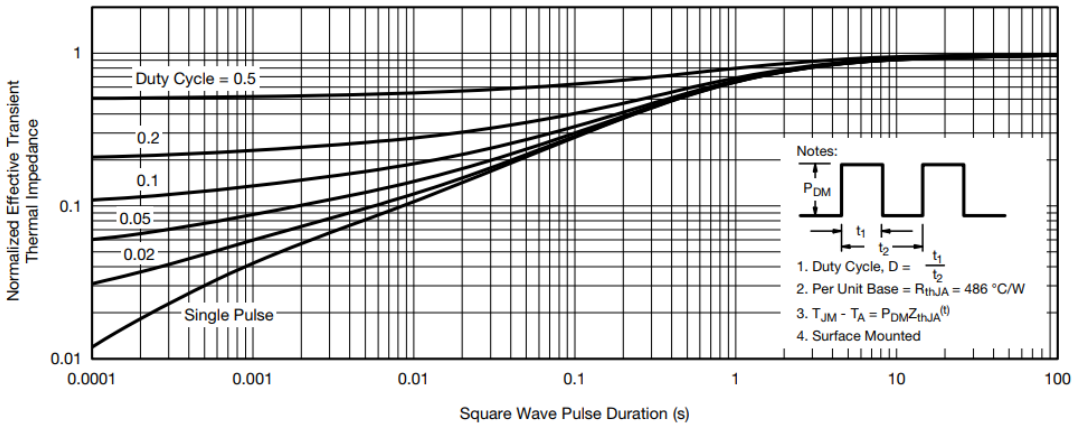
On-Resistance vs. Gate-to-Source Voltage



On-Resistance vs. Junction Temperature

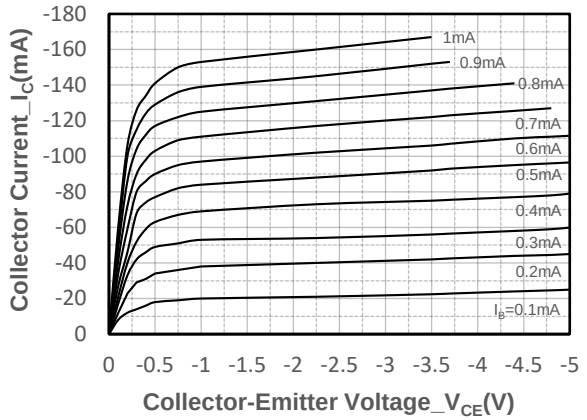


Safe Operating Area, Junction-to-Ambient

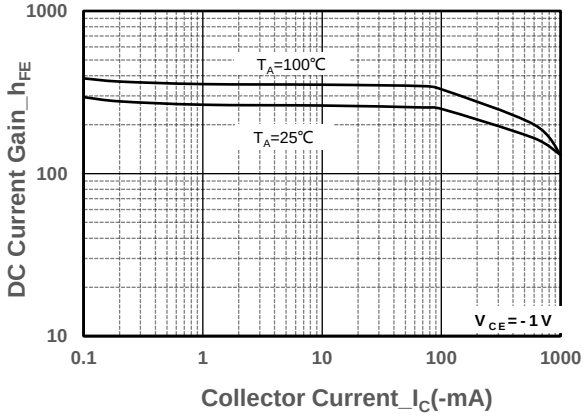


Normalized Thermal Transient Impedance, Junction-to-Ambient

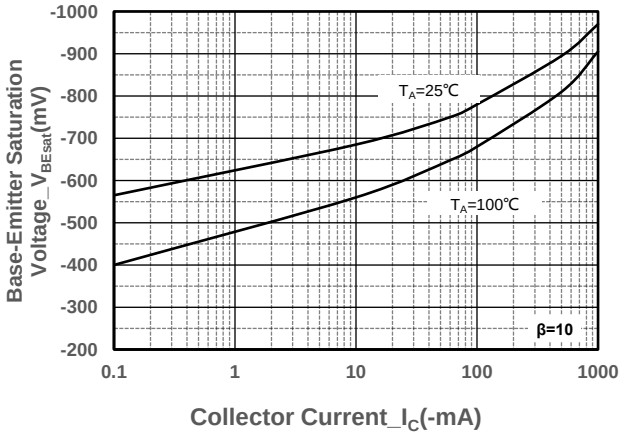
➢ PNP Transistor Typical Performance Characteristics (T_A=25℃)



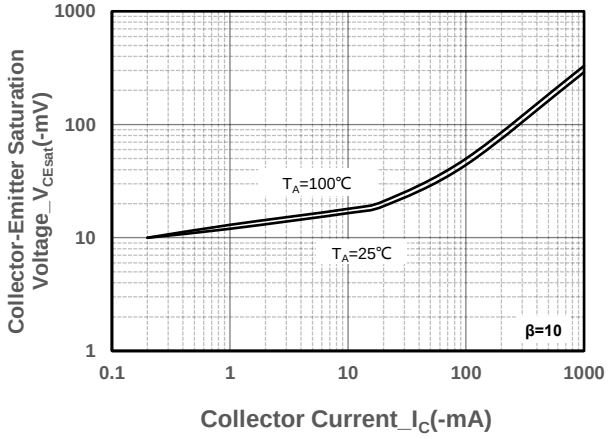
Collector Current vs. Collector-Emitter Voltage



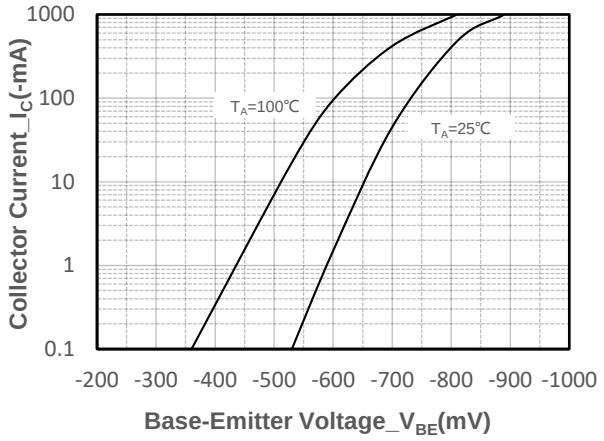
DC Current Gain vs. Collector Current



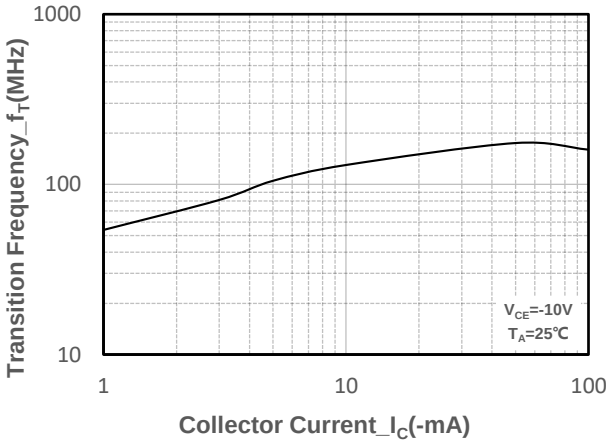
$V_{BE(sat)}$ vs. Collector Current



$V_{CE(sat)}$ vs. Collector Current

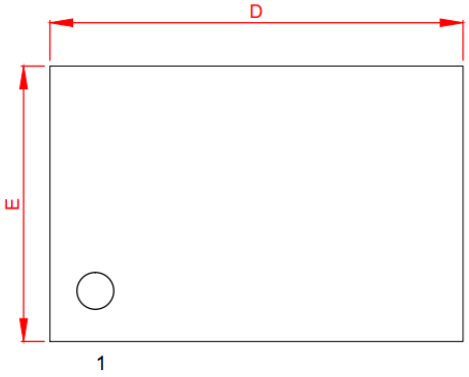


Collector Current vs. Base-Emitter Voltage

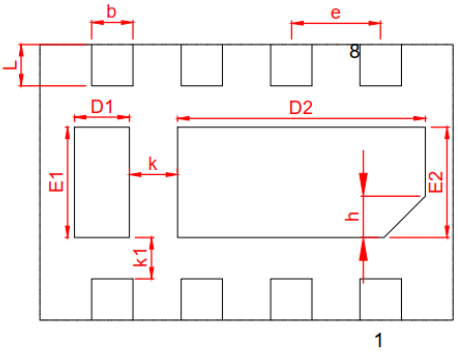


Transition Frequency vs. Collector Current

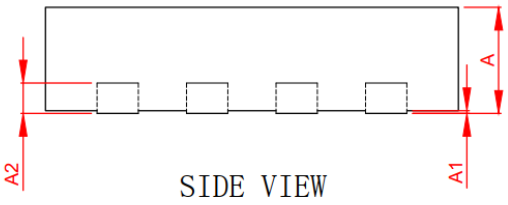
➢ Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
★ A1	0.00	0.02	0.05
★ b	0.25	0.30	0.35
A2		0.203 BSC	
★ D	2.90	3.00	3.10
★ E	1.90	2.00	2.10
★ E1	0.75	0.80	0.85
★ E2	0.75	0.80	0.85
★ D1	0.35	0.40	0.45
★ D2	1.75	1.80	1.85
★ e		0.65 REF	
★ L	0.25	0.30	0.35
h		BSC 0.42	
★ k1	0.30	0.35	0.40
★ k2	0.25	0.30	0.35

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